IN THE CLAIMS

Please amend Claims 1 and 2 as shown in marked-up form:

1. (Currently Amended) A method for testing digital circuitry ~~through~~ comprising:

effecting a paired loop-back from a first buffered output to a first buffered input;

~~-0whilst within the circuitry~~ executing at least part of the test through using a Built-In-Self-Test methodology within the circuity,

wherein the effecting step further comprises ~~characterized by~~ effecting said loop-back from the first buffered data output to a buffered control input, and wherein the method further comprises ~~in connection with said buffering,~~ executing a conversion step between a digital full swing internal signal and an analog low swing external signal and a conversion step between an analog low swing signal and a digital full swing signal, with respect to core circuitry of said digital circuitry.

2. (Currently Amended) A method for testing digital circuitry comprising:

~~through~~ effecting a paired data loop-back from a first buffered output to a first buffered input;

executing ~~whilst~~ within the circuitry ~~executing~~ at least part of the test through using a Built-In-Self-Test methodology,

wherein the effecting step further comprises ~~characterized by~~ effecting said loop-back from a buffered control output to the first buffered data input, and wherein the method further comprises in connection with said buffering, executing a conversion step between a digital full swing internal signal and an analog low swing external signal and a conversion step between an analog low swing signal and a digital full swing signal, with respect to core circuitry of said digital circuitry.

3. (Original) A method as claimed in Claim 1, characterized by effecting said loop-back from a buffered control output to the first buffered data input.

4. (Cancelled)

5. (Previously Presented) A method as claimed in Claim 1, wherein both said loop-back as well as said buffering are controlled through a one-bit control signal.

6. (Previously Presented) A method as claimed in Claim 5, wherein signal routing between said buffering on the one hand, and test circuitry as well as core circuitry of said digital circuitry, on the other hand, are controlled through a plural bit control signal.

C1

7-11 (Cancelled)